Dynamic Performance Improvement of Diode–capacitor-Based High Step-up DC–DC Converter Through Right-Half-Plane Zero Elimination

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Abstract—**Diode–capacitor-based dc–dc converters provide a simple and low cost solution for high step-up voltage regulation in solar and fuel cell generation. Transient modeling analysis reveals their worse influence of nonlinear and nonminimum-phase system characteristic due to right-half-plane (RHP) zero, especially in high voltage gain application. However, the process of energy transfer for diode–capacitor-based dc–dc converter is different from basic dc–dc converter. Based on the unique feature, this paper proposes an improved main circuit structure with parallel connection of resistive–capacitive damping network across the intermediate capacitor to achieve good dynamic performance. By optimal parameter design according to Routh–Hurtwiz criterion, all the RHP zeros in the transfer function of control-to-output voltage are eliminated completely. Then, by the case of diode–capacitor-based boost converter, the adaptive PI controller is designed to deal with nonlinear characteristic of voltage gain. It gets good dynamic performance under wide range output voltage. All the theoretical findings and design approaches are verified by simulation and experiment results. The existing diode–capacitor-based high step-up dc–dc converters with slight main circuit modification are more promising in renewable energy application.**

Index Terms—**Adaptive PI controller, diode-capacitor network, high voltage gain, resistive-capacitive damping network, right-half-plane (RHP) zero.**

I. Introduction

SOLAR and fuel cells are the most promising energy sources in the future for low environmental impact and scalability.

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However, unlike the conventional dc voltage source in power supply system, the obvious characteristic of them is low voltage supply with wide range voltage drop [1], [2]. In photovoltaic (PV) systems, it is difficult to realize a series connection of the PV cells without incurring a shadow effect. Fuel cells and light-weight battery power supply systems are promising in future hybrid electric vehicle, more-electric aircraft, and vessel. However, basic boost dc–dc converter is not able to achieve high voltage gain as well as high overall efficiency due to the parasitic parameters, and it has encountered the limitation of voltage regulation. Therefore, high step-up voltage regulation has become one of the key scientific and technical issues of power electronic converter with wide input voltage range, high efficiency, and high power density.

In order to achieve high voltage gain and avoid extremely large duty ratio, numerous novel nonisolated high step-up dc–dc topologies utilizing cascade structure, multilevel, coupling inductor, switch–capacitor/inductor network, and related control methods have been explored [2]–[18]. A family of high step-up dc–dc converter is proposed in [4]–[8], which introduces power diode and passive components to achieve high voltage gain. Fig. 1 shows the basic dc–dc converters and diode–capacitor-based high step-up dc–dc converters. The derived boost and buck-boost dc–dc converter composed of diode–capacitor network and the essential *LC* filter, shown in Fig. 1(b) and (d), provides a simple and effective approach to achieve high step-up ratio. Two intermediate capacitors are naturally charged in parallel during $S = $ OFF interval, and discharged in series during $S = $ ON interval. Compared with basic dc–dc converter, they have the following advantages [9]:

1) avoid extremely large duty ratio;
2) low voltage stress of switches which enables the use of low voltage rated and on-resistance power device;
3) small input and output current ripples which reduce the passive components requirement;
4) without introducing additional controllable power devices.

Furthermore, these topologies do not increase the complexity of control and drive circuit.

As for basic boost and buck-boost dc–dc converter operating under continues conduction mode, the control-to-output voltage
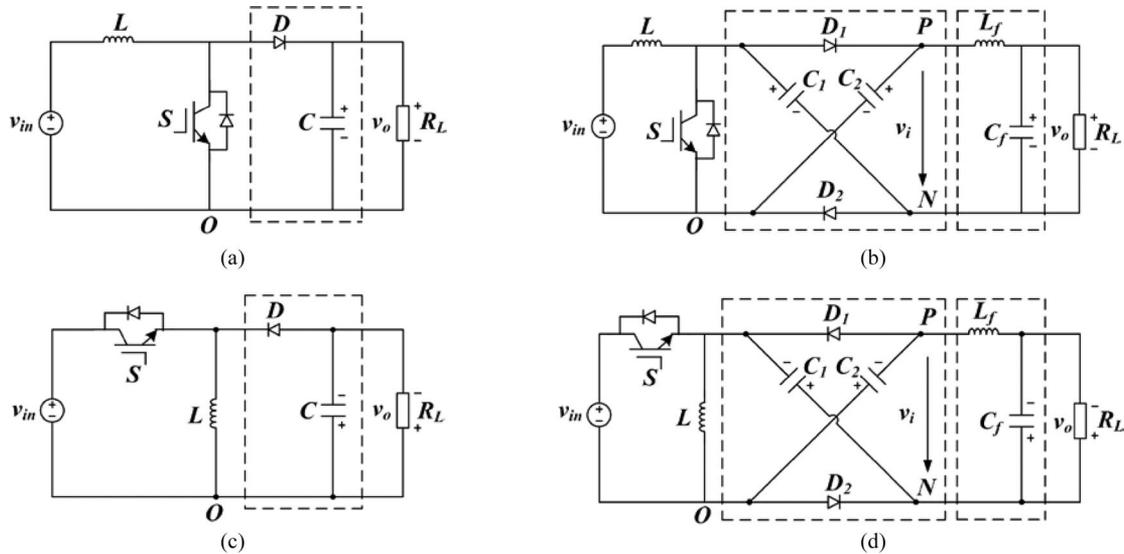
Fig. 1. Conventional dc–dc converters and diode–capacitor-based high step-up dc–dc converters. (a) Basic boost converter. (b) Diode–capacitor-based boost converter. (c) Basic buck-boost converter. (d) Diode–capacitor-based buck-boost converter.

transfer function contains a well-known right-half-plane (RHP) zero, which make a nonminimum phase system with relatively low bandwidth and slow dynamic performance. When the boost duty ratio steps up, more energy is stored in the inductor, rather than being transferred to the output side. Therefore, the output voltage initially decreases. In order to overcome the aforementioned limitation, Calvente *et al.* [13] first introduces an *LC* filter at the output side of basic dc–dc converter to attenuate both the switching noise and ripples, and then it utilizes the magnetically coupling combined with *RC*-type damping network to transfer the original RHP zeros to left-half-plane. The magnetic coupling between the input and output inductors allows the energy being transferred to the output side even if the output diode is turned OFF. The additional energy transfer channel explains the physical meaning of the RHP zeros elimination. However, the coupling inductor amplifies the input current ripples and increases current stress of the converter. Gu. *et al.* [14] presented the further input current ripples cancellation design approach for magnetic boost converter with an integrated three-winding couple inductor. The proposed integrated magnetic technique not only reduces the input and output current ripples but also solves the RHP zero issue. DC–DC converters with coupled inductor can achieve high step-up voltage gain and minimum phase system transfer function. However, the leakage inductance of couple inductor usually increases magnetic loss, voltage/current stress of power device, and cause more serious electromagnetic interface issue.

The RHP zero issue of basic dc–dc converter has been a hot research topic. However, this issue of diode–capacitor-based high step-up dc–dc converter has not been explored in the existing literature. As for diode–capacitor-based high step-up dc–dc converter shown in Fig. 1(b) and (d), during $S =$ ON interval, two intermediate capacitors are in series connection to supply the load. When the boost duty ratio increases, more energy in the intermediate capacitors is transferred to the output side. Obviously, the physical meaning of energy transfer process is totally different from basic dc–dc converter. Therefore, there may be

new method to deal with RHP zero issue for diode–capacitor-based high step-up dc–dc converter.

This paper first makes transient modeling analysis of diode–capacitor-based high step-up dc–dc converter in Section II. This nonminimum-phase system limits the voltage loop bandwidth and leads to worse dynamic influence, especially in high voltage gain application. In order to improve dynamic performance, this paper proposes a simple solution utilizing resistive–capacitive (*RC*-type) damping network to eliminate RHP zero and presents the detailed parameters design approach to achieve minimum phase transfer function in Section III. Based on this new topology, the adaptive PI controller is designed to achieve good dynamic performance under full operation range. Simulation and experiments verification are presented in Section IV. The conclusion of this study is outlined in Section V.

II. MODEL OF DIODE–CAPACITOR-BASED HIGH STEP-UP DC–DC CONVERTER

The state-space average and small-signal modeling technique gives a comprehensive method to study power electronic converter. It provides a good tool for better understanding of circuit performance and controller design.

A. Diode–Capacitor-Based Boost Converter

The aforementioned diode–capacitor-based high step-up dc–dc circuit has two operation modes according to the switching state of *S*. Fig. 2 shows two equivalent circuits. During $S =$ ON interval, the dc source transfers its electrostatic energy to magnetic energy stored in the inductor *L*. Both intermediate capacitors C_1 and C_2 are connected in series to charge the output capacitor C_f. During $S =$ OFF interval, the energy stored in *L* is transferred to C_1 and C_2, and both C_1 and C_2 are connected in parallel to charge the output capacitor C_f. For the convenience of analysis, C_1 and C_2 are assumed to have the same capacitance and terminal voltage [4], [5].
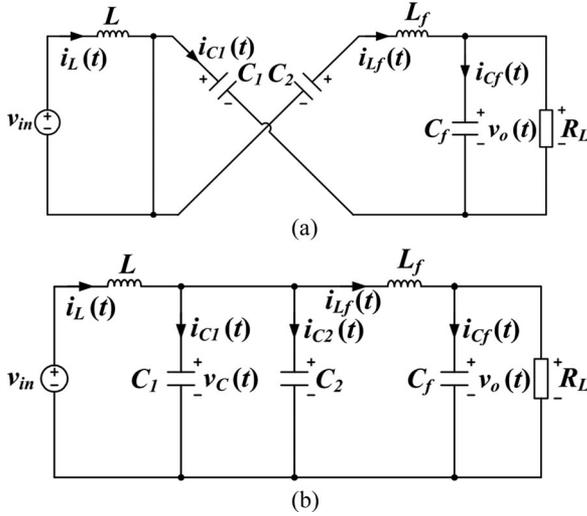
Fig. 2. Equivalent circuit of diode–capacitor-based boost converter. (a) During $S = $ ON interval. (b) During $S = $ OFF interval.

Taking all the inductor current (i_L, i_{Lf}) and capacitor voltage (v_C, v_{Cf}) as state variables, and using the state-space averaging method in one switching time period (T_s), the state equation can be expressed as

$$\begin{bmatrix} \dfrac{di_L(t)}{dt} \\ \dfrac{dv_C(t)}{dt} \\ \dfrac{di_{Lf}(t)}{dt} \\ \dfrac{dv_{Cf}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1-d(t)}{L} & 0 & 0 \\ \dfrac{1-d(t)}{2C} & 0 & -\dfrac{1+d(t)}{2C} & 0 \\ 0 & \dfrac{1+d(t)}{L_f} & 0 & -\dfrac{1}{L_f} \\ 0 & 0 & \dfrac{1}{C_f} & -\dfrac{1}{C_f R_L} \end{bmatrix}$$

$$\times \begin{bmatrix} i_L(t) \\ v_C(t) \\ i_{Lf}(t) \\ v_{Cf}(t) \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{\text{in}}. \tag{1}$$

From (1), the average model equivalent circuit of diode–capacitor-based boost converter is shown in Fig. 3. In these models, the control variable is d; the state variable to be controlled is output voltage v_{Cf}. The equilibrium operation point in steady state for fixed duty ratio $d = D$ is calculated by assuming the derivatives are zero

$$\begin{bmatrix} I_L \\ V_C \\ I_{Lf} \\ V_{Cf} \end{bmatrix} = \begin{bmatrix} \dfrac{(1+D)^2}{(1-D)^2} \cdot \dfrac{V_{\text{in}}}{R_L} \\ \dfrac{1}{1-D} \cdot V_{\text{in}} \\ \dfrac{1+D}{1-D} \cdot \dfrac{V_{\text{in}}}{R_L} \\ \dfrac{1+D}{1-D} \cdot V_{\text{in}} \end{bmatrix}. \tag{2}$$

The voltage gain of diode–capacitor-based boost converter is

$$G = \frac{v_o}{V_{\text{in}}} = \frac{1+D}{1-D}. \tag{3}$$

Performing small-signal perturbation at given equilibrium point (I_L, V_C, I_{Lf}, V_{Cf}) and ignore the high-order infinitesimals, the control-to-output voltage transfer function is

$$\frac{\hat{v}_{cf}(s)}{\hat{d}(s)} = \frac{a_2 \cdot s^2 + a_1 \cdot s + a_0}{b_4 \cdot s^4 + b_3 \cdot s^3 + b_2 \cdot s^2 + b_1 \cdot s + b_0} \tag{4}$$

where the numerator and denominator coefficients are

$$a_2 = \frac{2LCV_{\text{in}}R_L}{1-D}; \quad a_1 = -\frac{2LV_{\text{in}}(1+D)^2}{(1-D)^2}; \quad a_0 = 2R_L V_{\text{in}}$$

$$b_4 = 2LCL_f C_f R_L$$

$$b_3 = 2LCL_f$$

$$b_2 = \left[(1+D)^2 LC_f + 2LC + (1-D)^2 L_f C_f \right] R_L$$

$$b_1 = (1+D)^2 L + (1-D)^2 L_f$$

$$b_0 = (1-D)^2 R_L.$$

B. Diode–Capacitor-Based Buck-boost Converter

Using the similar derivation approach, the state equation of average model, the steady-state operation point, voltage gain, and the transfer function of control-to-output voltage perturbation for diode–capacitor-based buck-boost converter can be obtained as (5), (6), (7), and (8), respectively

$$\begin{bmatrix} \dfrac{di_L(t)}{dt} \\ \dfrac{dv_C(t)}{dt} \\ \dfrac{di_{Lf}(t)}{dt} \\ \dfrac{dv_{Cf}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1-d(t)}{L} & 0 & 0 \\ \dfrac{1-d(t)}{2C} & 0 & \dfrac{1+d(t)}{2C} & 0 \\ 0 & -\dfrac{1+d(t)}{L_f} & 0 & \dfrac{1}{L_f} \\ 0 & 0 & -\dfrac{1}{C_f} & -\dfrac{1}{C_f R_L} \end{bmatrix}$$

$$\times \begin{bmatrix} i_L(t) \\ v_C(t) \\ i_{Lf}(t) \\ v_{Cf}(t) \end{bmatrix} + \begin{bmatrix} \dfrac{d(t)}{L} \\ 0 \\ -\dfrac{d(t)}{L_f} \\ 0 \end{bmatrix} V_{\text{in}} \tag{5}$$

$$\begin{bmatrix} I_L \\ V_C \\ I_{Lf} \\ V_{Cf} \end{bmatrix} = \begin{bmatrix} \dfrac{2D(1+D)}{(1-D)^2} \cdot \dfrac{V_{\text{in}}}{R_L} \\ \dfrac{D}{1-D} \cdot V_{\text{in}} \\ -\dfrac{2D}{1-D} \cdot \dfrac{V_{\text{in}}}{R_L} \\ \dfrac{2D}{1-D} \cdot V_{\text{in}} \end{bmatrix} \tag{6}$$

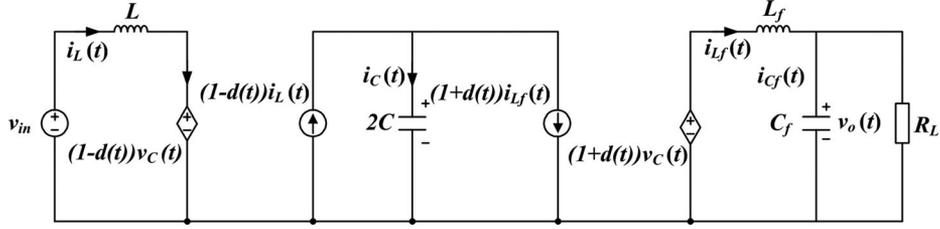$$G = \frac{v_o}{V_{\text{in}}} = \frac{2D}{1-D} \tag{7}$$

Fig. 3.   Average model equivalent circuit of diode–capacitor-based boost converter.
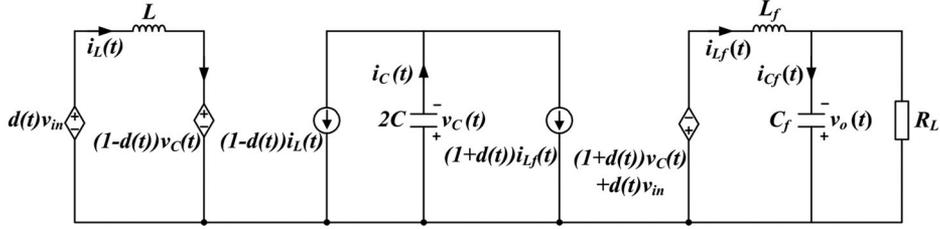

Fig. 4.   Average model equivalent circuit of diode–capacitor-based buck-boost converter.

$$\frac{\hat{v}_{cf}(s)}{\hat{d}(s)} = \frac{a_2 \cdot s^2 + a_1 \cdot s + a_0}{b_4 \cdot s^4 + b_3 \cdot s^3 + b_2 \cdot s^2 + b_1 \cdot s + b_0} \quad (8)$$

where the numerator and denominator coefficients are

$$a_2 = \frac{2LCV_{\mathrm{in}}R_L}{1-D}; a_1 = \frac{-4LV_{\mathrm{in}}D(1+D)}{(1-D)^2}; a_0 = 2R_L V_{\mathrm{in}}$$

$$b_4 = 2LCL_f C_f R_L; \; b_3 = 2LCL_f$$

$$b_2 = \left[(1+D)^2 LC_f + 2LC + (1-D)^2 L_f C_f \right] R_L$$

$$b_1 = (1+D)^2 L + (1-D)^2 L_f$$

$$b_0 = (1-D)^2 R_L.$$

From (5), the average model equivalent circuit of diode–capacitor-based buck-boost converter is shown in Fig. 4.

It can be observed in (4) and (8) that each of denominator coefficients is positive. However, one of the nominator coefficient a_1 is negative. Thus, the control-to-output voltage transfer function always contains a pair of conjugate RHP zeros. With RHP zeros, the output voltage falls before rising to the reference value when a step change of control command is given [19], and these RHP zeros are the cause of instability and limitation of closed-loop, therefore, the converter exhibits a worse dynamic performance like traditional boost dc–dc converter.

Root locus and bode diagram are the main methods for system characteristic analysis and controller design. The zero and pole locations of transfer function in S-domain move with the variations of main circuit parameters (L, L_f, C, C_f) and boost duty ratio d. These movements would result in unsatisfactorily oscillatory and worse nonminimum-phase responses especially in aforementioned renewable energy applications with the requirement of wide range voltage regulation. Therefore, it is necessary to study the movements of these zeros and poles to maintain acceptable performance and stability. To provide some insight of system parametric sensitivity, a group of root loci and bode plots are provided by changing a particular
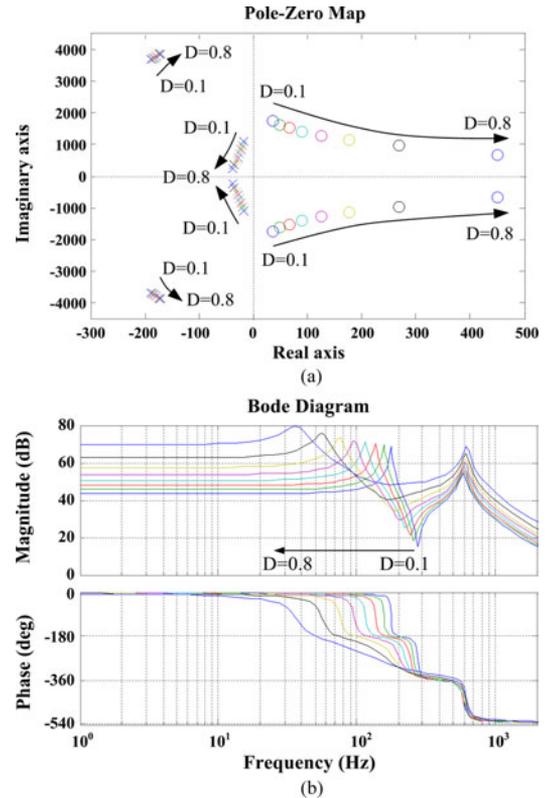

Fig. 5.   Frequency characteristic of control-to-output voltage perturbation in (4) with boost duty ratio variations. (a) Poles and zeros trajectories. (b) Bode diagram.

parameter with others kept constant. A practical analysis example was conducted with the following main circuit parameters and operation condition: $L = 2\,\mathrm{mH}$; $C_1 = C_2 = 150\,\mathrm{uF}$; $L_f = 4\,\mathrm{mH}$; $C_f = 20\,\mathrm{uF}$; $V_{\mathrm{in}} = 60\,\mathrm{V}$; $R_L = 120\,\Omega$. The capacitance and inductance are designed to accomplish the voltage and current ripples specification.

Fig. 5 shows the shifting of poles and zeros and the changing of bode diagram for the transfer function in (4) by varying the

boost duty ratio from 0.1 to 0.8. With increasing voltage gain, the locations of low-frequency poles are observed to move toward the real axis indicating an increase in system damping. The related first resonant peak is moving further to low frequency. It is noted that the scale of imaginary axis is much larger than that of real axis. Therefore, the locations of RHP zeros moving toward the real axis indicates the increase in nonminimum-phase under-shoot and oscillatory, while another pair of poles and the related location of high-frequency resonant peak almost remain unchanged. As is illustrated in Fig. 5(b), the conjugate poles and RHP zeros introduce 180° phase lag, respectively. However, the total phase lag has to be less than 180° at the crossing over frequency in order to guarantee the system stability. In general, for dc component control, the typical controller has to introduce an integrator to eliminate low frequency steady state error. It leads an additional 90° phase lag. The RHP zeros limit the bandwidth of voltage loop. In order to guarantee the system stability, typical voltage loop controller can not be designed well. The crossing over frequency has to be set at much small value, especially in high voltage gain application. The output voltage suffers long delay time and oscillatory response. Therefore, it is difficult to design voltage controller to meet the high performance requirement.

III. USING RESISTIVE-CAPACITIVE DAMPING TO ELIMINATE RHP ZEROS

The RHP zeros are the cause of instability and bandwidth limitation of closed-loop system. As is expressed in (4) and (8), the highest order term of the numerator coefficient a_2 is always positive and the passive components impedance L and C influence the location of RHP zeros. Both coefficients a_2 and a_1 contain L. In this case, RHP zeros always exist by changing the impedance of inductor. However, there is a possibility to change the equivalent impedance in the branch of intermediate capacitor by adding some passive network. The new main circuits for high step-up dc–dc converter are shown in Fig. 6. A series connection of a capacitor and a resistor is inserted in parallel connection with the intermediate capacitor. It provides another freedom to reset the location of zeros. For basic dc–dc converter, the highest order term of the numerator coefficient is always negative. Therefore, the RHP zeros cannot be eliminated by simply changing the passive components impedance in the main circuit.

With resistive–capacitive damping network shown in Fig. 7, the admittance of intermediate capacitor branch changes from sC to

$$Z_{im} = sC + \frac{sC_d}{1 + sC_d R_d}. \tag{9}$$

A. Diode–Capacitor-Based Boost Converter

As for high step-up dc–dc converter with *RC* damping network shown in Fig. 6(a), using the state-space averaging method in one switching time period (T_s), the state equation and the equilibrium operation point in steady state for fixed duty ratio
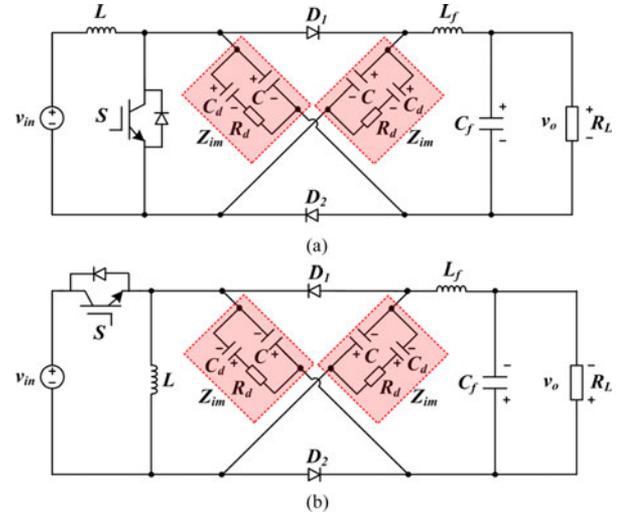

Fig. 6. High step-up dc–dc converter with resistive–capacitive damping network. (a) Diode–capacitor-based boost converter. (b) Diode–capacitor-based buck-boost converter.
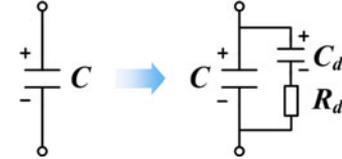

Fig. 7. Resistive–capacitive passive network.

$d = D$ is rewritten as

$$
\begin{bmatrix}
\dfrac{di_L(t)}{dt} \\[2mm]
\dfrac{dv_C(t)}{dt} \\[2mm]
\dfrac{dv_{Cd}(t)}{dt} \\[2mm]
\dfrac{di_{Lf}(t)}{dt} \\[2mm]
\dfrac{dv_{Cf}(t)}{dt}
\end{bmatrix}
=
$$

$$
\begin{bmatrix}
0 & -\dfrac{1-d(t)}{L} & 0 & 0 & 0 \\[2mm]
\dfrac{1-d(t)}{2C} & -\dfrac{1}{R_dC} & \dfrac{1}{R_dC} & -\dfrac{1+d(t)}{2C} & 0 \\[2mm]
0 & \dfrac{1}{R_dC_d} & -\dfrac{1}{R_dC_d} & 0 & 0 \\[2mm]
0 & \dfrac{1+d(t)}{L_f} & 0 & 0 & -\dfrac{1}{L_f} \\[2mm]
0 & 0 & 0 & \dfrac{1}{C_f} & -\dfrac{1}{C_fR_L}
\end{bmatrix}
$$

$$
\cdot
\begin{bmatrix}
i_L(t) \\
v_C(t) \\
v_{Cd}(t) \\
i_{Lf}(t) \\
v_{Cf}(t)
\end{bmatrix}
+
\begin{bmatrix}
\dfrac{1}{L} \\
0 \\
0 \\
0 \\
0
\end{bmatrix}
V_{\text{in}} \tag{10}
$$

$$\begin{bmatrix} I_L \\ V_C \\ V_{Cd} \\ I_{Lf} \\ V_{Cf} \end{bmatrix} = \begin{bmatrix} \dfrac{(1+D)^2}{(1-D)^2} \cdot \dfrac{V_{\text{in}}}{R_L} \\ \dfrac{1}{1-D} \cdot V_{\text{in}} \\ \dfrac{1}{1-D} \cdot V_{\text{in}} \\ \dfrac{1+D}{1-D} \cdot \dfrac{V_{\text{in}}}{R_L} \\ \dfrac{1+D}{1-D} \cdot V_{\text{in}} \end{bmatrix}. \tag{11}$$

From (2), (3), and (11), the improved main circuit structure of high step-up dc–dc converter with *RC* damping network has the same voltage gain and steady-state operation point.

Substituting Z_{im} into (4) to replace sC, the boost duty ratio to output voltage transfer function for diode–capacitor-based boost converter with resistive–capacitive (*RC-type*) damping network can be written as

$$\frac{\hat{v}_{cf}(s)}{\hat{d}(s)} = \frac{a_3 \cdot s^3 + a_2 \cdot s^2 + a_1 \cdot s + a_0}{b_5 \cdot s^5 + b_4 \cdot s^4 + b_3 \cdot s^3 + b_2 \cdot s^2 + b_1 \cdot s + b_0} \tag{12}$$

where the numerator and denominator coefficients are

$$a_3 = \frac{2V_{\text{in}}}{(1-D)} L C R_L R_d C_d$$

$$a_2 = \frac{2LV_{\text{in}}}{(1-D)} \left[R_L(C + C_d) - R_d C_d \frac{(1+D)^2}{(1-D)} \right]$$

$$a_1 = 2C_d R_d R_L V_{\text{in}} - 2LV_{\text{in}} \frac{(1+D)^2}{(1-D)^2}$$

$$a_0 = 2R_L V_{\text{in}}$$

$$b_5 = 2LCL_f C_f R_L C_d R_d$$

$$b_4 = [2CC_d R_d + (1+D)C_f R_L C_d + 2CC_f R_L] L L_f$$

$$b_3 = 2LCC_d R_d R_L + [(1+D)^2 L + (1-D)^2 L_f]$$
$$\times\ C_f R_L C_d R_d + [(1+D)C_d + 2C] L L_f$$

$$b_2 = [(1+D)^2 L + (1-D)^2 L_f](C_f R_L + C_d R_d)$$
$$+\ [(1+D)LC_d + 2LC] R_L$$

$$b_1 = [(1+D)^2 L + (1-D)^2 L_f] + C_d R_d R_L (1-D)^2$$

$$b_0 = (1-D)^2 R_L.$$

Applying the Routh–Hurwitz criterion to the numerator polynomial of (12), the following conditions have to be satisfied in order to ensure all the zeros located in the left half-plane

$$a_0 > 0;\ a_1 > 0;\ a_2 > 0;\ a_3 > 0;\ a_1 a_2 - a_0 a_3 > 0. \tag{13}$$

The passive components parameters in (12) are fixed. Evidently, $a_0 > 0$ and $a_3 > 0$ always stand. The converter provides adjustable output voltage under different load resistor R_L. Fig. 8 shows three curves of a_1, a_2, and $a_1 a_2 - a_0 a_3$ under different R_L. a_1 and a_2 are the linear functions of load resistance R_L with positive slope and $a_1 a_2 - a_0 a_3$ is parabola
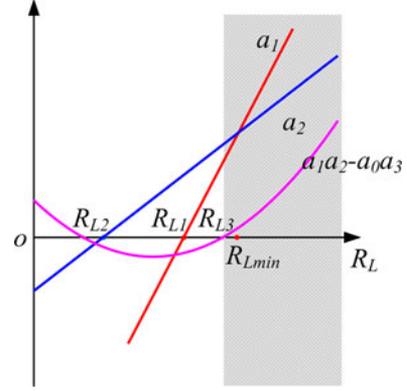

Fig. 8. Relationship of coefficients a_1, a_2, and $a_1 a_2 - a_0 a_3$ versus R_L.

function of R_L. Inequalities (13) are simultaneously satisfied if R_L is larger than R_{L3}, in which, the following critical condition R_{L1}, R_{L2} and R_{L3} can be obtained by assuming $a_1 = 0$; $a_2 = 0$; $a_1 a_2 - a_0 a_3 = 0$, respectively

$$R_{L1} = \frac{(1+D)^2 L}{(1-D)^2 R_d C_d} \tag{14}$$

$$R_{L2} = \frac{R_d C_d (1+D)^2}{(C + C_d)(1-D)} \tag{15}$$

$$R_{L3} = \frac{C + C_d}{C_d} \left(\frac{R_{L1} + R_{L2}}{2} \right.$$
$$\left. + \sqrt{ \left(\frac{R_{L1} - R_{L2}}{2} \right)^2 + \frac{LC(1+D)^4}{(1-D)^3 (C + C_d)^2} } \right). \tag{16}$$

Due to $R_{L2} \leq R_{L1} < R_{L3}$ from (16), once the load resistance meets the condition of $R_L \geq R_{L3}$, as the shadow area shown in Fig. 8, $a_1 > 0$, $a_2 > 0$, $a_1 a_2 - a_0 a_3 > 0$ are simultaneously satisfied. From (16), there is optimal parameters design of *RC* damping network to minimize R_{L3} when $R_{L1} = R_{L2}$. The optimal *RC* damping network meets

$$R_d = \frac{1}{C_d} \sqrt{ \frac{(C + C_d)L}{1 - D} }. \tag{17}$$

Substituting R_d expressed in (17) into (16), R_{L3} is rewritten as

$$R_{L3} = \frac{(1+D)^2}{\sqrt{C + C_d} - \sqrt{C}} \sqrt{ \frac{L}{(1-D)^3} }. \tag{18}$$

The minimum phase transfer function should be designed to guarantee the maximum output power when the load resistance achieves minimum $R_{L\min}$, which means $R_{L3} < R_{L\min}$. Calculated from (18), the intermediate C_d and C meet the following equation:

$$C_d \geq \frac{(1+D)^4 L}{(1-D)^3 R_{L\min}^2} + \frac{2(1+D)^2 \sqrt{LC(1-D)}}{(1-D)^2 R_{L\min}} \tag{19}$$

Based on (17) and (19), the main circuit parameters of diode–capacitor-based boost dc–dc converter without RHP zeros can

be well designed. This minimum-phase system is beneficial to increases the closed-loop bandwidth. It allows the simplified design of voltage regulator with good dynamic behavior.

B. Diode–Capacitor-Based Buck-boost Converter

Similarly, substituting Z_{im} into (8) to replace sC, for diode–capacitor-based buck-boost converter without RHP zeros shown in Fig. 6(b), the transfer function of boost duty ratio to output voltage, the optimal RC-type damping network parameters R_d and C_d are expressed as follows:

$$\frac{\hat{v}_{cf}(s)}{\hat{d}(s)} = \frac{a_3 \cdot s^3 + a_2 \cdot s^2 + a_1 \cdot s + a_0}{b_5 \cdot s^5 + b_4 \cdot s^4 + b_3 \cdot s^3 + b_2 \cdot s^2 + b_1 \cdot s + b_0} \tag{20}$$

where the numerator and denominator coefficients are

$$a_3 = \frac{2V_{\text{in}}}{1-D} LCR_L R_d C_d$$

$$a_2 = \frac{2V_{\text{in}}L}{1-D}\left[R_L(C + C_d) - \frac{2R_d C_d D(1+D)}{1-D}\right]$$

$$a_1 = 2C_d R_d R_L V_{\text{in}} - \frac{4LV_{\text{in}}D(1+D)}{(1-D)^2}$$

$$a_0 = 2R_L V_{\text{in}}$$

$$b_5 = 2LCL_f C_f R_L C_d R_d$$

$$b_4 = 2LL_f(CC_d R_d + C_d C_f R_L + CC_f R_L)$$

$$b_3 = 2LCC_d R_d R_L + C_f R_L C_d R_d[(1+D)^2 L$$
$$\quad + (1-D)^2 L_f] + 2LL_f(C_d + C)$$

$$b_2 = [(1+D)^2 L + (1-D)^2 L_f](C_f R_L + C_d R_d)$$
$$\quad + 2LR_L(C_d + C)$$

$$b_1 = [(1+D)^2 L + (1-D)^2 L_f] + C_d R_d R_L(1-D)^2$$

$$b_0 = (1-D)^2 R_L$$

$$R_d = \frac{1}{C_d}\sqrt{\frac{L(C+C_d)}{1-D}} \tag{21}$$

$$C_d \geq \frac{4D^2(1+D)^2 L}{(1-D)^3 R_{L\,\text{min}}^2} + \frac{4D(1+D)}{(1-D)^2 R_{L\,\text{min}}}. \tag{22}$$

IV. SIMULATION AND EXPERIMENT VERIFICATION

To verify above novel high step-up dc–dc main circuit structure without RHP zeros, a practical design example of diode–capacitor-based boost converter was conducted. The main circuit specifications and operation condition are $L = 2\,\text{mH}$; $L_f = 4\,\text{mH}$; $C_f = 25\,\mu\text{F}$; $V_{\text{in}} = 60\text{–}90\,\text{V}$; $V_o = 120\text{–}240\,\text{V}$; $R_L = 80\text{–}160\,\Omega$; $f_s = 10\,\text{kHz}$. According to (17) and (19), $C = 20\,\mu\text{F}$, $C_d = 150\,\mu\text{F}$ and $R_d = 4.2\,\Omega$ has been chosen with a sufficient margin. Compared with the main circuit parameters listed in Section II, in order to eliminate RHP zeros,
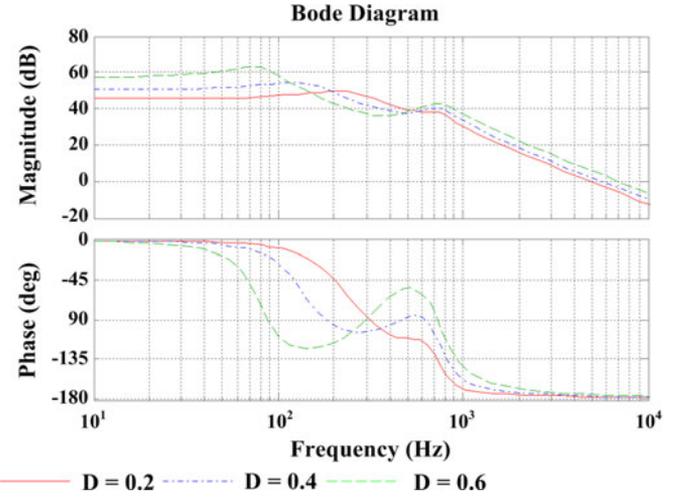

Fig. 9. Frequency characteristic of control to output voltage perturbation with different boost duty ratio.
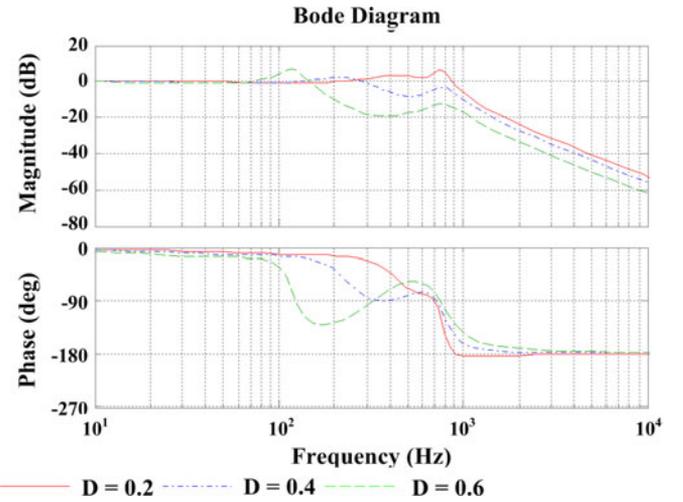

Fig. 10. Frequency characteristic of closed-loop transfer function with different controller parameters.

the modified main circuit introduces a much small capacitor and resistor, which may not increase system cost significantly.

In above operation conditions, the maximum boost duty ratio is $d = 0.6$. The corresponding frequency characteristic of control to output voltage transfer function under different boost duty ratio is shown in Fig. 9. Compared with the bode diagram of the existing topology shown in Fig. 5(b), the new circuit introduces RC-type damping to smooth the resonate peak and valley, which helps to reduce the oscillatory response. Furthermore, the minimum phase system provides certain phase margin for adequate bandwidth design, and the total phase lag is 180°. As shown in Fig. 9, the frequency characteristic exhibits evident discrepancy in magnitude and phase curves under different boost duty ratio due to nonlinear relationship of voltage gain. In general, the compensator should be designed to obtain a stable dynamic response under the worst case. The typical PI compensator expressed as (23) needs to provide sufficient magnitude and phase margin under the maximum boost duty ratio $d = 0.6$. However, it may deteriorate the dynamic response when the boost
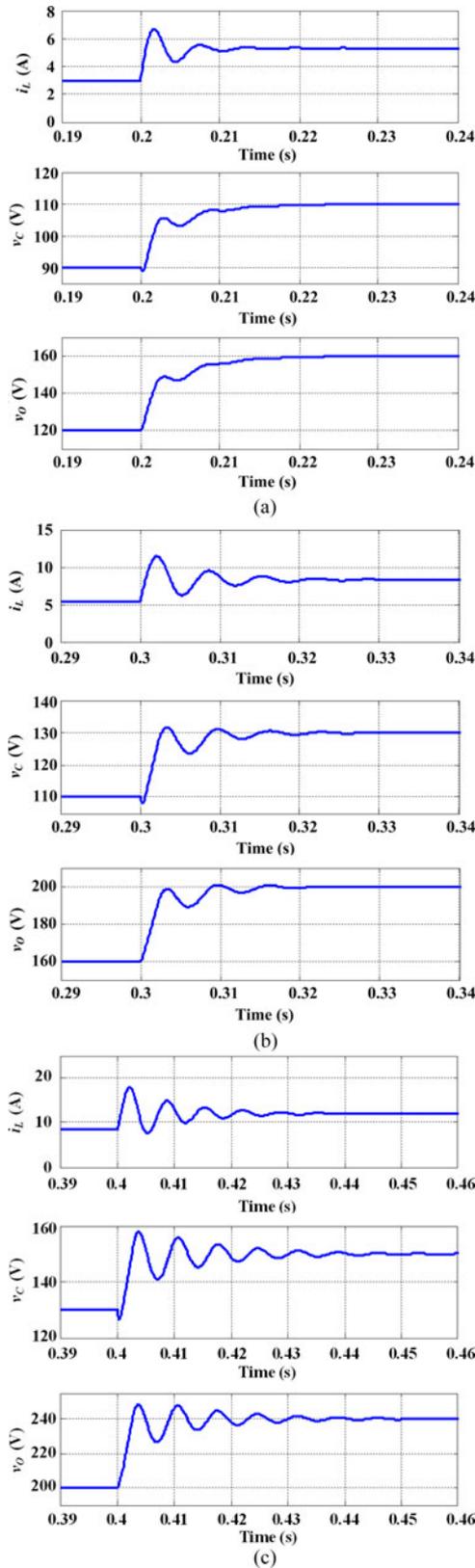
Fig. 11. Waveforms of new main circuit with fixed PI parameter under different step change of reference. (a) Step change of reference voltage from 120 to 160 V. (b) Step change of reference voltage from 160 to 200 V. (c) Step change of reference voltage from 200 to 240 V.
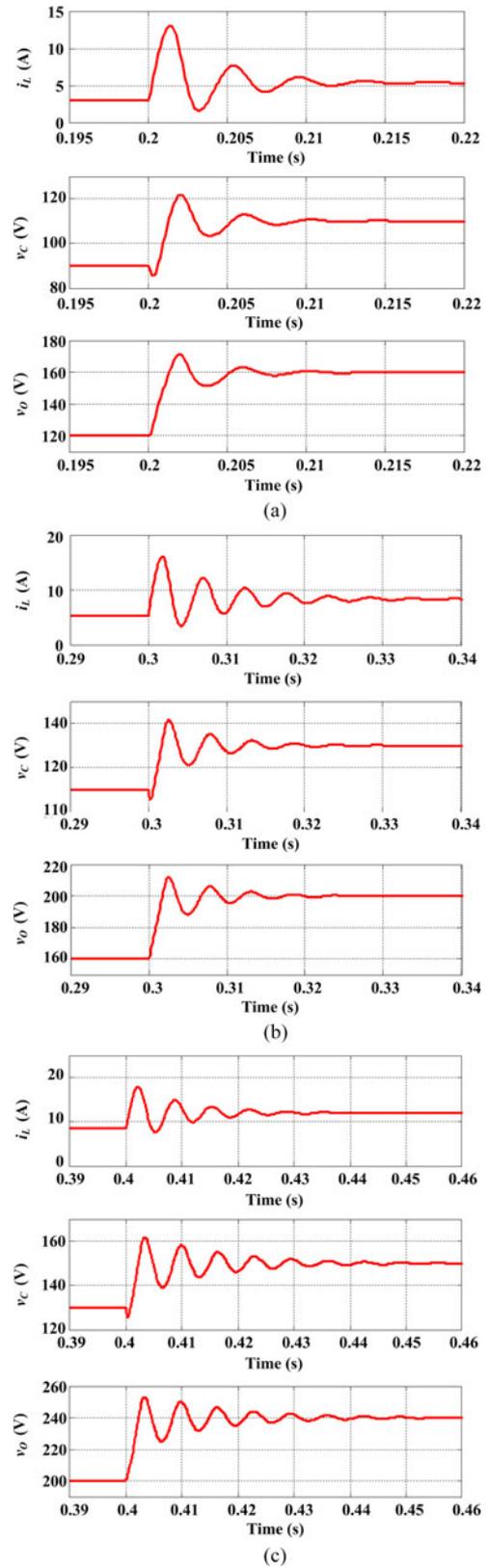

Fig. 12. Waveforms of new main circuit with adaptive PI parameters under different step change of reference. (a) Step change of reference voltage from 120 to 160 V. (b) Step change of reference voltage from 160 to 200 V. (c) Step change of reference voltage from 200 to 240 V.
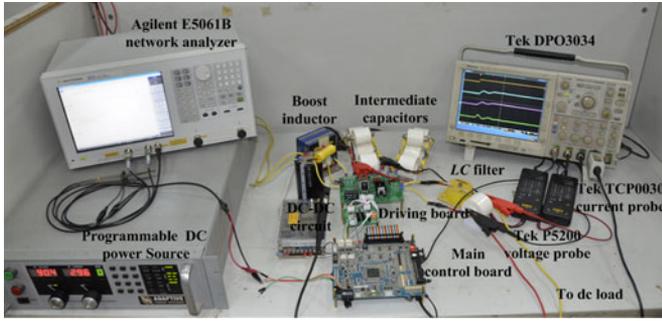
Fig. 13. Test platform of high step-up dc–dc converter with diode–capacitor network.
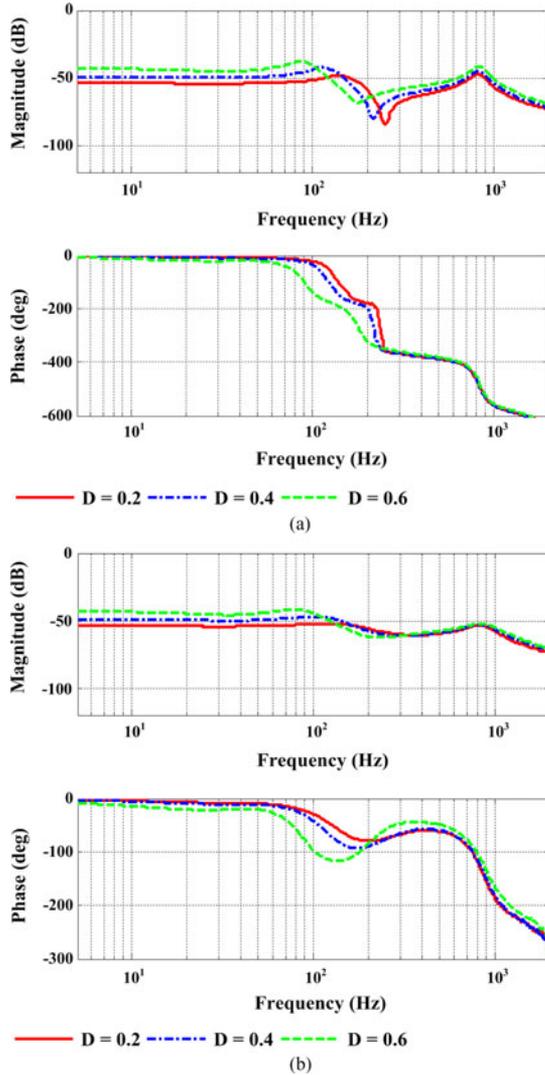

D = 0.2   D = 0.4   D = 0.6

(a)

D = 0.2   D = 0.4   D = 0.6

(b)

Fig. 14. Frequency characteristic of the boost duty ratio to output voltage transfer function. (a) Without RC-type damping network. (b) With RC-type damping network.

(a)

(b)

Fig. 15. Output voltage response of diode–capacitor-based high step-up dc–dc converter without RC-type damping network. (a) Step-up of duty ratio D from 0.4 to 0.6. (b) Step-down of duty ratio D from 0.6 to 0.4.

(a)

(b)

Fig. 16. Output voltage response of diode–capacitor-based high step-up dc–dc converter with RC-type damping network. (a) Step-up of duty ratio D from 0.4 to 0.6. (b) Step-down of duty ratio D from 0.6 to 0.4.

converter operates under the relatively low voltage gain

$$C_{pi} = K_p + K_i T_s \frac{z}{z-1}. \tag{23}$$

Gain scheduling [20] is usually used in designing a nonlinear controller, which adjusts the controller gain along with the
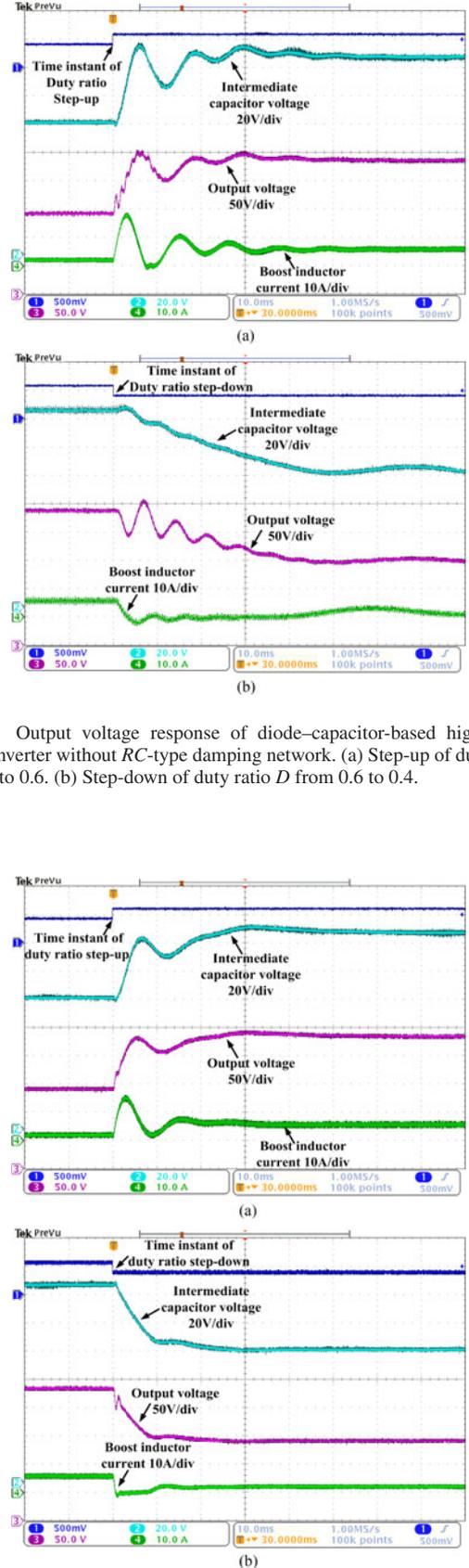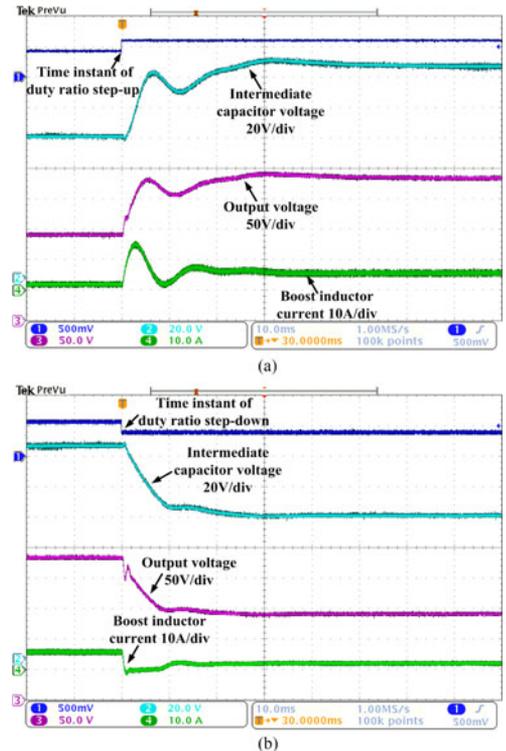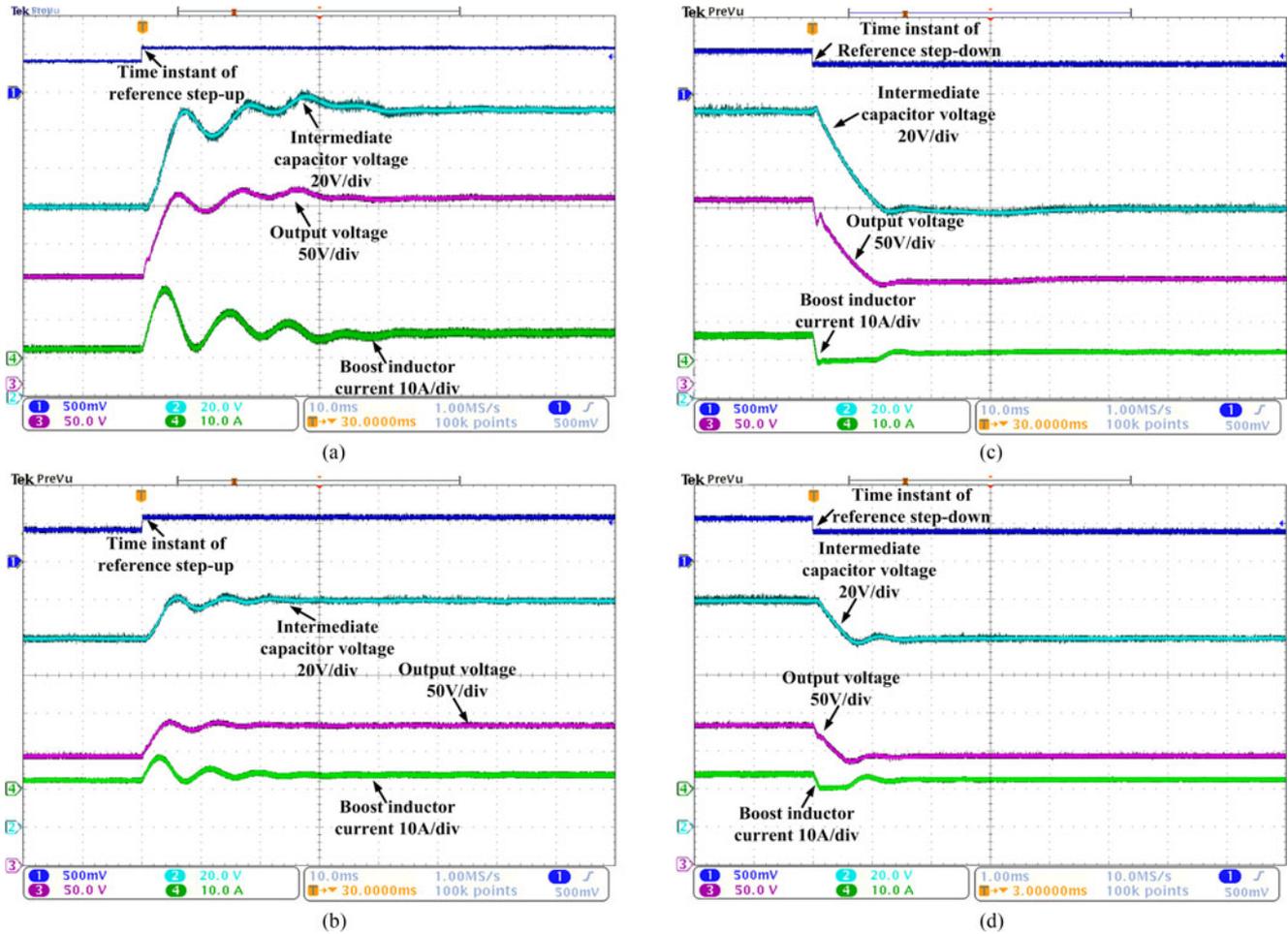
Fig. 17. Waveforms of diode–capacitor-based high-step up dc–dc converter under step change of reference voltage with closed-loop controller. (a) Step-up of V_{ref} from 140 to 240 V. (b) Step-down of V_{ref} from 240 to 140 V. (c) Step-up of V_{ref} from 140 to 180 V. (d) Step-down of V_{ref} from 180 to 140 V.

operation point. In the first, three groups of PI controller parameters are designed to meet the corresponding magnitude and phase margin at different steady-state operation points. $C_{pi(D\,=\,0.2)} = 0.97 + 0.145 \cdot z/(z-1)$; $C_{pi(D\,=\,0.4)} = 0.504 + 0.042 \cdot z/(z-1)$; $C_{pi(D\,=\,0.6)} = 0.164 + 0.012 \cdot z/(z-1)$. Fig. 10 shows the frequency characteristic of closed-loop transfer function for high step-up dc–dc converter operating under three equilibrium boost duty ratio with the optimal controller parameters. The corresponding crossing-over frequency is almost 800, 200, and 100 Hz, respectively.

Fig. 11 shows the simulation waveforms of diode–capacitor-based boost converter with fixed PI controller parameters under different step change of the output reference. As shown in Fig. 11, the PI controller designed under the maximum boost duty ratio is very stable and gets good dynamic performance in high output voltage application. Furthermore, the step response of output voltage does not suffers any undershoot, which means complete elimination of RHP zeros in the system. However, when the converter requires wide range voltage regulation, the output voltage response is comparatively slow in low voltage gain application.

The linear first-order polynomial approximation is obtained from a series of PI parameters using curve fitting. The controller utilizes the polynomial to adjust the PI parameters based on the targeted voltage gain. With adaptive controller, the boost converter is able to get good dynamic response under full operation range. Fig. 12 shows the related simulation waveforms of boost inductor current, intermediate capacitor voltage, and output voltage with adaptive PI controller under the same step change of reference. With gain scheduling controller, the optimal PI parameters are utilized and the output voltage response is always fast with acceptable overshoot. The diode–capacitor-based high step-up dc–dc converter exhibits good dynamic performance under full operation range.

Efficiency is an important criterion for dc–dc converter in solar and fuel cell generation. Compared with basic boost dc–dc converter, diode–capacitor-based high step-up dc–dc converters demonstrate obvious advantages in efficiency in high voltage gain application. The additional loss introduced by the resistors in *RC*-type damping network is analyzed. In steady-state operation, the capacitance of C is far smaller than C_d, which means that almost all the switching current

flows through C, and the ac current across R_d is very small. Therefore, with optional design of RC-type damping network, the converter efficiency does not deteriorate in a practical implementation.

A laboratory prototype rated at 1 kW with the same main circuit and controller parameters in the simulation is built to verify the aforementioned theoretical analysis. The main control board is designed based on TMS320F28335. Fig. 13 shows the photo of test platform. A programmable dc power supply is arranged as dc source to simulate the V–I characteristics of fuel stacks or solar arrays. The network analyzer Agilent E5061 is implemented for frequency characteristic measurement. The injection source of network analyzer generates sweeping sinusoidal signal of controllable amplitude and frequency. TMS320F28335 samples the small ac signal $\hat{d}$ and injects it into boost duty ratio. At the same time, Agilent E5061 measures output voltage disturbance $\hat{v}_o$ and displays the magnitude and phase characteristic of $\hat{v}_o/\hat{d}$.

Fig. 14 shows the measured frequency characteristic curves of main circuit without and with RC-type damping network. Obviously, after introducing RC-type damping network, the 180° phase delay is extend from 100 to 1000 Hz, which provide the enough phase margin to meet the voltage loop bandwidth requirement. The measured experiments results verify that high step-up dc–dc converter with RC-type damping network eliminate RHP zeros and simplify the controller design.

Figs. 15 and 16 show the measured waveforms for high step-up dc–dc converter with open loop controller under the step change of boost duty ratio. Without RC-type damping network, the output voltage has some initial time delay and obvious oscillatory process. Thus, it enters the new state after a long time. However, with RC-type damping network, the output voltage of the proposed converter rises up immediately, since no previous RHP zero exists. The response is fast and the system oscillation is depressed to a great extent. Furthermore, both converters have the same voltage boost capability and output voltage in steady state.

The closed-loop voltage controller is designed with adjustable parameter based on different operation condition. Fig. 17 shows the measured waveforms for high step-up dc–dc converter with single-loop voltage controller under the step change of output voltage reference. The control to output minimum phase system is beneficial to eliminate the potential unstable factors. The proposed high step-up dc–dc converter demonstrates the improved system stability and dynamic performance, especially in high voltage gain application.

V. Conclusion

This paper starts by transient modeling of diode–capacitor-based high step-up dc–dc converter. The frequency characteristic analysis reveals this nonminimum-phase system leads to undesired dynamic performance, especially in high voltage gain application. Then, the RC-type damping network in parallel connection of intermediate capacitor is applied to transfer all the zeros to left-half-plane. With some slight modification based on the existing high step-up dc–dc circuits, the new main circuit struc-

ture present the advantages of minimum phase control-to-output transfer function and simplified closed-loop controller design. Both advantages are promising for dc–dc converter with fast response. With adaptive PI controller, diode–capacitor-based high step-up dc–dc converters demonstrate good steady-state and transient performance.

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